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EXAMINER	
BEVERIDGE, RACHEL E	
ART UNIT	PAPER NUMBER
1725	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/722,432	Applicant(s) KWARK ET AL.	
	Examiner Rachel E. Beveridge	Art Unit 1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 November 2003_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

4a) Of the above claim(s) _25 and 26_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-5, 7-15, 17, 19-21, 23-24, and 27-30_ is/are rejected.

7)☒ Claim(s) _6,16,18 and 22_ is/are objected to.

8)☒ Claim(s) _1-30_ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _28 November 2003_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _01/06/2004_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

The examiner withdraws the previous species restriction. For the current action the examiner examined claims 1-24 and 27-30. Claims 25-26 are restricted and were withdrawn from examination.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 2A(207) and 2B(207). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 6, 16, 18, and 22 are objected to but would be allowable if the independent claim 1 and dependent claim 5 were allowable.

Regarding claim 6, prior art shows continuous dielectric material surrounding bonding wires; however, the periodic placement of dielectric material around bonding wires was not found in prior art and is therefore in condition for allowance if the independent claim 1 and dependent claim 5 were allowable.

Regarding claim 16, no prior art was found disclosing a plurality of bonding wires for signal transmission comprising a coplanar waveguide or similar structure fitting the applicant's definition of coplanar waveguide. Therefore, the claim is in condition for allowance if the independent claim 1 was allowable.

Regarding claim 18, no prior art was found disclosing a differential signal via a plurality of bonding wires. Therefore, the claim is in condition for allowance if the independent claim 1 was allowable.

Regarding claim 22, prior art was found to show effect of an impedance transformer (see discussion of claim 21); however, due to the claims dependence on claim 6, no prior art was found to include the effect with respect to the periodic placement of dielectric material around bonding wires. Thus, the claim is in condition for allowance if the independent claim 1 and dependent claims 5-6 were allowable.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. "A combination of at least one round bonding wire and at least one ribbon wire" fails to point out whether applicant is claiming a combination of round wire and ribbon wire, a combination of only round wires, or a combination of only ribbon wires. For examination purposes, the examiner interpreted the claim to be a combination of only round wires.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 9, 12, 14, 19, 24, and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

With respect to claim 1, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor

chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

With regard to claim 2, Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1. Regarding claim 3, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

Regarding claim 4, Horiuchi discloses a ground potential of the signal wire and dielectric insulation (column 5, lines 22-27). Regarding claim 5, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33).

With respect to claim 7, Horiuchi teaches the resin coating (32) to cover the bonding section and an electro-conductive resin (34) used for shielding (column 6, lines 14-17). Figure 3 also shows an epoxy type coating (30) on a gold wire (28) to be the bond wire (20) connecting the signal between semiconductor and circuit board. With respect to claim 9, Horiuchi also shows wires in a predetermined configuration alongside one another in figures 7(a) and 8.

With regard to claim 12, Horiuchi's figure 3 shows a round bonding wire. With regard to claim 14, the examiner interpreted the claim to be a combination of only round wires. Horiuchi's figure 3 shows a round bonding wire.

Regarding claim 19, the examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of

specified values for a high dielectric constant. Horiuchi discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33) and that an electro-conductive resin (34) is capable of easily shielding the semiconductor chip (10) (column 5, lines 34-37). Horiuchi also discloses the lack of risk of a short-circuit between the bonding wires (20) even though they are shielded with electro-conductive resin (34) because the electrode terminals and bonding section between the wires (20) and pads (22) are covered with electro-insulation resin (32) (column 5, lines 37-44).

With respect to claim 24, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33).

Regarding claim 27, Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54). Horiuchi teaches a plurality of bonding wires (20) with conductive wire and electro-insulation coating for electrically connecting the circuit board (5) to the semiconductor chip (10) (column 2, lines 1-9). Horiuchi also discloses matching the impedance to that of a signal line by selecting the insulation material (column 5, lines 29-33). Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.

With respect to claim 28, the examiner interpreted the claim to have controlled impedance designed near in value to an impedance of a circuit to which the signal line is interconnected with the chip circuit. Horiuchi discloses electrically connecting a semiconductor chip (10) to a connection (12) on a circuit board (5) (column 5, lines 51-54).

With regard to claim 29, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33). Figures 8 and 9 clearly show a predetermined pattern and distance between the wires (42) with dielectric material (40) surrounding them. Horiuchi also teaches carefully selecting the dielectric material for the dielectric constant "and/or" thickness (column 5, lines 34-37).

Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Notani et al. (US 5,294,897). Notani discloses the reduction of the reflection of high frequency signals caused by the mismatching of characteristic impedances in the transmission line (column 6, lines 6-9). Notani also discloses a transmission line with continuous transmission between the lines and the circuit package substrate (column 5, lines 34-40). Furthermore, Notani shows a plurality of bonding wires in figures 1(a), 4(b), 6, 7, 8, and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 5 above, and further in view of Chia et al. (US 2004/0182911 A1). Horiuchi teaches epoxy as insulation but lacks disclosure of the type of epoxy used for the invention. Chia teaches wire bonding utilizing an insulating liquid (112), more specifically using ultra-violet light-cured epoxies (Chia et al., page 1, paragraph [0021], lines 3-4). Therefore, it would have been obvious to one of ordinary skill the art at the time of the invention to modify the wire bonding method of Horiuchi to utilize the ultra-violet light-cured epoxy of Chia in order to electrically insulate the bonding wires and attach them to the package in any desired sequence without causing package defects (Chia et al., page 2, paragraph [0026], lines 3-7).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Steranko et al. (US 3,840,169). With respect to claim 10, Horiuchi teaches dispensing wires for bonding but lacks disclosure of co-dispensing a plurality of bonding wires. However, Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. Regarding claim 11, Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material

(dielectric constant) and/or thickness of the resin coating *32* covering the conductive wire" (column 5, lines 29-33). Figures 8 and 9 clearly show a predetermined pattern and distance between the wires (42) with dielectric material (40) surrounding them. Horiuchi also teaches carefully selecting the dielectric material for the dielectric constant "and/or" thickness (column 5, lines 34-37). However, Horiuchi lacks disclosure of co-dispensing a plurality of bonding wires. Steranko discloses bonding multiple wires to a circuit board continuously (abstract, lines 1-9) as shown in figure 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the co-dispensing apparatus of Steranko in order to have strong bonding of multiple wires at one time (Steranko et al., column 1, lines 40-44).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Lee (US 2001/00154900 A1). Horiuchi discloses bonding a plurality of bonding wires for signal transmission between and semiconductor chip (10) and a circuit board (5). However, Horiuchi lacks bonding a plurality of ribbon wires in the package. Lee teaches ribbon bonding wire for signal transmission (page 3, paragraph [0031], lines 3-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the bonding of ribbon bonding wire between the chip and circuit board in order to model transverse distribution adequately and utilize a wire-grid method to understand the influence of material during

signal transmission (Lee, page 3, paragraph [0031], lines 6-10, and paragraph [0030}, lines 4-6).

Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 1 above, and further in view of Notani et al. (US 5, 924,897). With respect to claim 15, Horiuchi lacks specific description of the bonding wires to comprise a microstrip. Notani discloses a transmission line having a microstrip line structure (column 7, lines 1-2). Regarding claim 17, it is understood that a microstrip transmits a single-ended signal as disclosed by the applicant. Therefore, Notani's disclosure of a transmission line having a microstrip structure (column 7, lines 1-2) satisfies a single-ended signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the disclosed microstrip of Notani in order to arrange the strip signal conductor opposite a ground conductor on the dielectric (Notani et al., column 7, lines 2-3).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 19 above, and further in view of Kurtz et al. (US 4,555,052). The examiner interpreted high to be any value for dielectric constant of the insulating material due to the lack of relation to a low value and lack of specified values for a high dielectric constant. Horiuchi lacks disclosure of the particular material comprising the dielectric. However, Kurtz discloses ceramic as a dielectric material useful for electric insulation (column 6, lines 52-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire

bonding method of Horiuchi to include the ceramic dielectric of Kurtz in order to properly bond the wire for transmission while the package is grounded (Kurtz et al., column 6, lines 47-52).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 19 above, and further in view of Lee (US 2001/0015490 A1). Horiuchi lacks disclosure of the spacing of the dielectric particles ability to specifically affect a filter or impedance transformer. Lee discloses results on analysis of the dielectric material for input impedances and effective parasitic inductances versus frequencies of different wire bonding combinations (page 4, paragraph [0043]). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to disclose the dielectrics spacing relative to the effect of an impedance transformer in order to cause a reduction of reduction reactance from the offset of inductive reactance prevalent in the bonding wire due to capacitive reactance from the dielectrics wide range of frequencies (Lee, page 4, paragraph [0044], lines 16-22).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. (US 6,084,295) as applied to claim 28 above, and further in view of Notani et al. (US 5,294,897). Horiuchi lacks specific description of the bonding wires to comprise a microstrip. Notani discloses a transmission line having a microstrip line structure (column 7, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the wire bonding method of Horiuchi to include the

disclosed microstrip of Notani in order to arrange the strip signal conductor opposite a ground conductor on the dielectric (Notani et al., column 7, lines 2-3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachel E. Beveridge whose telephone number is (571) 272-5169. The examiner can normally be reached on Monday through Friday, 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on (571) 272-1292. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

REB

JONATHAN JOHNSON
PRIMARY EXAMINER